REMARKS

The specification has been amended to correct minor typographical errors. Accordingly, the Applicant respectfully requests that the above amendments to the specification be approved. The Applicant submits that no new matter has been added by virtue of the above amendments to the specification.

Claims 1-22 are rejected under 35 U.S.C. Section 103(a) as allegedly being unpatentable over by U.S. Patent No. 5,604,514 to Hancock ("Hancock '514") in view of U.S. Patent No. 5,699,277 to Munson et al. ("Munson '277"), further in view of U.S. Patent No. 5,666,137 to Coelho et al. ("Coelho '137"), and further in view of U.S. Patent 5,526,025 to Selwan et al. ("Selwan '025"). The Applicant respectfully traverses this rejection for the reasons presented below.

As amended, independent claim 1 now recites a display controller that includes:

> bus interface means, coupled to the data bus, for receiving video data in a component YUV format and corresponding video data addresses within a predetermined address range; and
>
> a ***display memory controller***, coupled to said bus interface means, for receiving video data in a

component YUV format in contiguous successive streams of luminance and chrominance difference data and corresponding video data addresses within a predetermined address range and ***for storing said video data by directing separate luminance and chrominance difference data into predetermined memory portions according to a predetermined memory aperture mapped to a display memory so as to store said video data in a pixel video format in the display memory.*** (emphasis added)

The claimed invention includes a display memory controller "for receiving video data in a component YUV format in contiguous successive streams of luminance and chrominance difference data and corresponding video data addresses within a predetermined address range and ***for storing said video data by directing separate luminance and chrominance difference data into predetermined memory portions according to a predetermined memory aperture mapped to a display memory so as to store said video data in a pixel video format in the display memory***". The claimed invention beneficially provides a display controller that can assist a host processor in decoding MPEG data. The display controller receives YUV data in non-pixel video format from a host CPU and performs the otherwise CPU intensive task of rasterization. Thus, the

display controller beneficially takes the rasterization chore away from an MPEG decoder in the host processor by making clever use of memory apertures to store the data directly into video pixel. Additionally, the memory aperture used to store data is "a hitherto unused display memory address aperture" and thus the display controller can maintain compatibility with the PCI bus standard and prior art display controller software and hardware." (see specification, page 20, lines 11-15).

The claimed invention is not disclosed or suggested by Hancock '514, Munson '277, Coelho '137, and Selwan '025, either alone or in combination. Hancock '514 discloses a video subsystem 16 that includes a video memory access controller 28, a video memory 30, a video display controller 32, a DAC 34, and a monitor 36. (col. 3, lines 25-29). The video memory access controller 28 provides pixel data values and pixel state values to the video memory 30 (see Fig. 1 of Hancock '514). The video memory 30 comprises a pixel data region 38 and a pixel state mask 40 defining the state of each pixel, and the controller 32 continuously accesses the pixel data in video memory 30 one pixel at a time and decides the color for a pixel. (col. 3, lines 34-36 and col. 4, lines 7-9). The pixel state mask determines how the video controller 32 is to interpret the pixel data for that pixel and thus

allows the concurrent display of graphics and image data. (col. 2, lines 49-53). Hancock '514 does not disclose, as recited in claim 1, a display memory controller ***for storing said video data by directing separate luminance and chrominance difference data into predetermined memory portions according to a predetermined memory aperture mapped to a display memory so as to store said video data in a pixel video format in the display memory.***

The Examiner correctly states that Hancock '514 fails to expressly teach a bus interface means coupled to the data bus. In an attempt to overcome the deficiency of Hancock '514, the Examiner relies on Munson '277 to show a bus interface means (PIB) 109 coupled to a PCI bus 115.

However, combining Hancock '514 with Munson '277 would not yield the Applicant's claimed invention. As stated above, Hancock '514 discloses a video memory access controller 28 for providing pixel data values and pixel state values to the video memory 30. On the other hand, Munson '277 discloses a method and apparatus for coupling a video camera to a host computer for transmitting video images therebetween. (col. 3. lines 46-48). In particular, Munson '277 discloses an embodiment 100 that "serves as the interface between a National Television Standards Committee (NTSC)/Phase

Alternation Line (PAL)/SECAM digital video decoder/scaler 117 and a Peripheral Component Interconnect (PCI) local bus 115 of a personal computer." (col. 5, lines 58-63). The PCI interface block (PIB) 109 "operates as a PCI bus master when the video DMA controller [106] is delivering captured video images to the PCI memory 111, the RPS 108 is accessing PCI memory 111 for register value lists or writing data, and the DCI block 103 is fetching data." (col. 26, lines 25-33). The combination of Hancock '514 and Munson '277 does not yield the Applicant's claimed invention, since neither reference discloses the Applicant's recited display memory controller ***for storing said video data by directing separate luminance and chrominance difference data into predetermined memory portions according to a predetermined memory aperture mapped to a display memory so as to store said video data in a pixel video format in the display memory***.

The Examiner also correctly states that Munson '277 fails to expressly teach a receiving method of video data in contiguous successive streams of luminance and chrominance difference data. In an attempt to overcome the deficiency of Munson '277, the Examiner relies on Coelho '137 to show a "technique for formatting YUV9 subsampled data as known in the art (byte lane arrangement), wherein a frame buffer is divided

into plural blocks for storing sequential packed video stream data (Y,U,V)." (see Office Action, page 3).

Coelho '137 discloses a method for converting planar YUV data into a "packed" (interleaved) YUV format whereby a videoprocessor 302 converts the planar YUV data into the packed YUV data. In the packed format, a frame of the planar data is divided into blocks. (col. 2, lines 37-41). A first block B11 has the transmitted color and intensity data in the following format (V11, U11, Y11, Y12, Y13, Y13, Y21, Y22, Y23, Y24, Y31, Y32, Y33, Y34, Y41, Y42, Y43, Y44). The data for block B12 is subsequently transmitted in a corresponding format (V15, U15, Y15, Y16, Y17, Y18, Y25, Y26, Y27, Y28, Y35, Y36, Y37, Y38, Y45, Y46, Y47, Y48). This pattern of data transmission is followed from left to right in Band 1 (Fig. 1) and then is continued from left to right in Band 2, and to subsequent bands until the entire frame of YUV data is transmitted. (col. 2, lines 42-60). The videoprocessor 302 then sends the packed YUV data to a digital graphics display controller 304 which sends a corresponding analog RGB signal to a video display monitor 305. (col. 4, lines 2-9).

The Applicant submits that isolated disclosures in the prior art cannot be combined where there is no suggestion or incentive to do so. The CAFC has repeatedly noted that:

> Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination. Under Section 103, teachings of references can be combined only if there is some suggestion or incentive to do so. The prior art of record fails to provide any such suggestion or incentive. (Emphasis original). ACS Hospital Systems, Inc. v. Montefiore Hospital, 231 U.S.P.Q. 929, 933 (C.A.F.C. 1984).

In the instant case there is not suggestion or incentive to combine Hancock '514, Munson '277, and Coelho '137 as the Examiner has suggested. Once cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to duplicate the claimed invention.

Assuming for the sake of argument that there is a suggestion to combine, the combination of Hancock '514, Munson '277, and Coelho '137 does not equal the claimed invention. The combination of Hancock '514, Munson '277, and Coelho '137 provides, at best, a system that includes a video memory access controller for providing pixel data values and pixel state values to a video memory, and that further includes a video processes for converting planar YUV data into "packed" (interleaved) YUV format. Thus, the combination of Hancock

'514, Munson '277 and Coelho '137 does not yield the Applicant's claimed invention, since the Applicant recites in claim 1, a display memory controller ***for storing said video data by directing separate luminance and chrominance difference data into predetermined memory portions according to a predetermined memory aperture mapped to a display memory so as to store said video data in a pixel video format in the display memory,*** and no such display memory controller is described in any of the prior art.

The Examiner also correctly states that the references of Hancock '514, Munson '277, and Coelho '137 fail to teach a bit block transfer engine for performing a replicating function. (see Office Action, page 3). In an attempt to overcome the above deficiency, the Examiner relies on Selwan '025 to show an apparatus and method "for performing run length tagging by the use of BITBLT circuit (1106), BITBLT tag generation circuit block (1202), FIFO controller (1220) sending a signal on bus (1228) to alert display memory controller (1210) to stop loading data at FIFO full condition". (see Office Action, pages 2-3).

Fig. 11 in Selwan '025 discloses a VGA accelerator display controller that includes a CPU bus interface and write buffer 1102, a graphics controller 1104, a BITBLT and FIFO

block 1106, a CRT controller block 1108, and a display memory sequencer block 1110. The display memory sequencer block 1110 further comprises a display memory controller 1122. Data is sent from BITBLT and FIFO block 1106 to display memory controller 1122. The pixel FIFO 1124 (in display sequencer block 1110) receives data bursts from a display memory through display memory controller 1122 which are to be output to the CRT. (col. 17, lines 58-66).

The combination of Hancock '514, Munson '277, Coelho '137, and Selwan '025 does not yield the Applicant's claimed invention, since the Applicant recites in claim 1, a display memory controller ***for storing said video data by directing separate luminance and chrominance difference data into predetermined memory portions according to a predetermined memory aperture mapped to a display memory so as to store said video data in a pixel video format in the display memory.***

As amended, independent claim 12 now recites a method for assisting decoding of video data partially decoded in a host processor, comprising the steps of:

> receiving, in a display controller, video data in a component YUV format in contiguous successive streams of luminance and chrominance difference data and

corresponding video data addresses within a predetermined address range, and

storing the video data by directing separate luminance and chrominance difference data into predetermined memory portions according to a predetermined memory aperture mapped to a display memory so as to store said video data in a pixel video format in the display memory. (emphasis added).

As stated above, Hancock '514 discloses a video memory access controller 28 that provides pixel data values and pixel state values to a video memory 30. The controller 32 continuously accesses the pixel data in video memory 30 one pixel at a time and decides the color for a pixel. (col. 3, lines 34-36). Hancock '514 does not disclose, as recited in claim 12, the step of ***storing the video data by directing separate luminance and chrominance difference data into predetermined memory portions according to a predetermined memory aperture mapped to a display memory so as to store said video data in a pixel video format in the display memory***

For the same reasons stated above, Hancock '514, Munson '277, Coelho '137, and Selwan '025, either alone or in combination, do not yield the Applicant's claimed invention which includes the step of ***storing the video data by directing***

separate luminance and chrominance difference data into predetermined memory portions according to a predetermined memory aperture mapped to a display memory so as to store said video data in a pixel video format in the display memory. For example, the combination of Hancock '514, Munson '277, and Coelho '137 provides, at best, a method that includes the steps of storing pixel data and pixel state values in a video memory by use of a video memory access controller, using a video display controller to continuously access the pixel data in the video memory one pixel at a time, and converting planar YUV data into a "packed" (interleaved) YUV format.

Since dependent claims 2-11 and 13-22 depend from various ones of claims 1 and 12 and include all limitations thereof, the dependent claims also patentably distinguish over Hancock '514, in view of Munson '277, further in view of Coelho '137, and further in view of Selwan '025, for at least the same reasons that independent claims 1 and 12 distinguish over the same references. The patentability of claims 2-11 and 13-22, however, does not depend on the patentability of their respective base claims, inasmuch as each dependent claim recites an additional feature which, in combination with the features recited in the base claims, are not disclosed by the cited references. For example, dependent claim 2 recites the

video data as comprising luminance and chrominance difference data and the component YUB format as comprising a first contiguous block of luminance data and at least a second contiguous block of chrominance difference data. The above feature of dependent claim 2 is not recited in the above cited references.

The Applicant respectfully submits that claims 1-22 are now patentably distinguishable from the cited reference. In view of the above claim amendments and remarks, the applicant respectfully requests allowance of claims 1-22.

The Applicant also hereby requests and petitions for an extension of time of one (1) month for responding to the Office Action dated May 12, 1998. Attached herewith is a Petition For Extension Of Time and a check in the amount of $110.00 for the requisite extension fee.

Respectfully submitted,

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